MULTIPROGRAMMER INTERFACE

MODEL 59500A

OPERATING AND SERVICE MANUAL

FOR SERIALS 1544A-00123 AND ABOVE *

* For Serials Above 1544A-00123
a change page may be included.

* For Serials Below 1544A-00123
Refer to Appendix A.

TABLE OF CONTENTS

1-1   SCOPE

1-2   This instruction manual provides operating and service instructions for Multiprogrammer Interface, Model 59500A. The 59500A is designed specifically to permit bi-directional operation of the 6940B Multiprogrammer and any 6941B Multiprogrammer Extenders on the Hewlett-Packard Interface Bus (HP-IB).

1-3   Procedures for operating and programming the multiprogrammer system (59500A, 6940B, 6941B) on the HP-IB, under control of an HP programmable calculator (9830A or 9820A/21A) are provided in the 6940B Multi-programmer User's Guide. Operating and service instructions for the 6940B and 6941B are provided in separate service manuals. All related publications are listed in Paragraph 1-10.

1-4   The purpose of this manual, therefore, is to provide all of the information necessary to service the 59500A unit. Refer to the 6940B Multiprogrammer User's Guide for system programming and installation instructions.

1-5   DESCRIPTION

1-6   The 59500A buffers and transmits data and control signals between the HP-IB and the 6940B. It converts the serial ASCII alphanumerics of the HP-IB to the 16-bit parallel format required by the 6940B Multiprogrammer. The 59500A also adapts the 3-wire handshake process used on the HP-IB to the 2-wire method (Gate/Flag) employed by the 6940B.

1-7   The 59500A's interface circuits are contained on a multilayer printed circuit board which contains over 60 integrated circuits. Operating voltage for the interface circuits is provided by a +5V regulated power supply equipped with crowbar protection. HP-IB and multiprogrammer interface connectors are located on the rear of the 59500A unit. Table 1-1 lists general information regarding operation of the 59500A on the HP-IB.

1-8   HP-IB COMPATIBILITY

1-9   The 59500A/6940B can function on the HP-IB as a talker or as a listener and has source handshake, acceptor handshake, and service request capabilities. The 59500A/6940B does not have: controller, device clear, device

trigger, extended listener, parallel poll, remote/local, and extended talker HP-IB capabilities. Refer to Section III for descriptions of each function.

1-10   RELATED PUBLICATIONS

1-11   The 6940B Multiprogrammer User's Guide for the HP-IB (59500-90003) provides all of the information required to install, program, and use the multiprogrammer system (6940B/6941B, 59500A) on the HP-IB with a calculator (9830A, or 9820A/21A). The 59500-90003 User's Guide includes basic circuit descriptions and verification procedures for the 6940B Multiprogrammer and 59500A Interface units.

1-12   Detailed operating and servicing instructions for the 6940B and 6941B mainframes are provided in Operating and Service Manuals 06940-90005 and 06941-90003, respectively. Operating and Service Manuals are also provided for each type of mainframe plug-in card (Models 69321 through 69601). Programming examples (using 9830 or 9820A/21A) for each type of card are provided in Chapter VI in the 59500-90003 User's Guide.

1-13   Calculator publications include the HP-IB User's Guides (59300-90002 for the 9830A and 59300-90001 for the 9820A/21A) and Operating and Programming Manuals (09830-90001 or 09820-90001).

1-14   INSTRUMENT IDENTIFICATION

1-15   Hewlett-Packard instruments are identified by a three-part serial number. The first part is the instrument model number. The second part is the serial number prefix, consisting of a number-letter combination denoting the date of a significant design change and the country of manufacture. The first two digits indicate the year (14=1974, 15=1975, 20=1980, etc.); the second two digits indicate the week (01 through 52); and the letter "A", "G", "J", or "U" designates the U. S. A., West Germany, Japan, or the United Kingdom, respectively, as the country of manufacture. The third part is the instrument serial number; a different 5-digit sequential number is assigned to each instrument, starting with 00101.

1-16   If the serial number prefix on your unit does not agree with the prefix on the title page of this manual, change sheets supplied with the manual define the differences

between your instrument and the instrument described by this manual.

1-17 ORDERING ADDITIONAL MANUALS

One manual is shipped with each instrument. Additional manuals may be purchased from your local Hewlett-Packard field office (see list at rear of this manual for addresses). Specify the model number, serial number prefix, and HP part number shown on the title page.

Table 1-1. General Information

ELECTRICAL CHARACTERISTICS

Logic Levels: Ground true, TTL compatible.
Input Levels (From HP-IB):
    1 = true $\leqslant 0.8V$
    $\emptyset$ = false $\geqslant 2.0V$
Output Levels (To HP-IB):
    1 = true = 0Vdc to 0.4Vdc
    $\emptyset$ = false = +2.5Vdc to +5Vdc

Input Loading (From HP-IB): Each of the 16 bus lines is terminated with 3kΩ to +5V and 6.2kΩ to ground. Each input is equivalent to one TTL load (or less).

Output Circuits (To HP-IB): Each of 11 open collector output circuits (DIO1-DIO7, SRQ, DAV, NRFD, NDAC) can drive 14 bus loads.

Input Loading (From 6940B): Each of 16 inputs $\overline{B15}$, $\overline{B11}$-$\overline{B\emptyset\emptyset}$, $\overline{FLAG}$, $\overline{TME}$, $\overline{IEN}$) is terminated with 330Ω to +5V and 750Ω to ground.

Output Circuits (To 6940B): 17 open collector drivers for data bits $\overline{D\emptyset\emptyset}$-$\overline{D15}$ and $\overline{GATE}$ signal.

FUNCTION

Interfaces the 6940B Multiprogrammer to the controller and up to 13 additional bus devices via the HP-IB. Provides the following HP-IB capabilities: talker (T6), listener (L4), source handshake (SH1), acceptor handshake (AH1), and service request (SR1).

Interconnecting Cables:
    (1)   Controller-to-59500A: Standard 72-inch (1.8 meters) HP-IB cable No. 10631B, supplied with 59500A.

    (2)   59500A-to-6940B: Standard 18-inch (0.46 meters) chaining cable No. 14541A, supplied with 59500A.

Operating Modes:
    (1)   Listen mode: 59500A can input data from the HP-IB when addressed.

    (2)   Talk mode: 59500A can output data to the HP-IB when addressed.

    (3)   Service request: 59500A can notify the controller that the 6940B requires service. The service request (SRQ) line allows a single bus instrument to request service while the calculator is doing another operation.

Talk/Listen Addresses:
    The 59500A/6940B Multiprogrammer has a suggested talk address of "W" and listen address of "7" which are factory set (address switches on rear of 59500A). However, any of 31 pairs of talk/listen address combinations can be selected using the address switches on rear of 59500A.

Connectors:
    (1)   The HP-IB connector (24-pins) is located on the rear of the 59500A and is designated J1.
    (2)   The MULTIPROGRAMMER connector (50-pins) is located on the rear of the 59500A and is designated J2.

INPUT POWER REQUIREMENTS

100/120/220/240Vac (selectable), 48-440Hz, 15W.

TEMPERATURE RANGE:

Operating: $0°$ to $55°C$.
Storage: $-40°$ to $+75°C$

59500A DIMENSIONS:

3 1/4 inches (82.6mm) high x 16 3/4 inches (425.5mm) wide x 18 3/4 inches (463.6mm) deep.

59500A WEIGHT:

12 lbs. (5.4kg)

COOLING:

Natural Convection.

SECTION II
INSTALLATION

2-1   INITIAL INSPECTION

2-2   Before shipment, this instrument was inspected and found to be free of mechanical and electrical defects. As soon as the instrument is received, proceed as instructed in the following paragraphs.

2-3   Mechanical Check

2-4   If external damage to the shipping carton is evident, ask the carrier's agent to be present when the instrument is unpacked. Check the instrument for external damage such as broken controls or connectors, and dents or scratches on the panel surfaces. If the instrument is damaged, file a claim with the carrier's agent and notify your local Hewlett-Packard Sales and Service Office as soon as possible (see list at rear of this manual for addresses).

2-5   Electrical Check

2-6   Check the electrical performance of the instrument as soon as possible after receipt. Section V of this manual contains procedures which will verify instrument operation on the HP-IB. These procedures are also suitable for incoming quality control inspection. Refer to the inside front cover of the manual for the Certification and Warranty statements.

2-7   REPACKAGING FOR SHIPMENT

2-8   To insure safe shipment of the instrument, it is recommended that the package designed for the instrument be used. The original packaging material is reusable. If it is not available, contact your local Hewlett-Packard field office to obtain the materials. This office will also furnish the address of the nearest service office to which the instrument can be shipped. Be sure to attach a tag to the instrument specifying the owner, model number, full serial number, and service required, or a brief description of the trouble.

2-9   INSTALLATION DATA

2-10   HP-IB Connector

2-11   The HP-IB connector (J1) on the rear of the 59500A interfaces directly to the HP-IB. Figure 2-1 illustrates the pin configuration of J1 which is a 24-pin, type 57, micro-

ribbon connector. The HP-IB cable, supplied with the 59500A, is 6 feet in length. HP-IB cables are also available in 3 feet and 12 feet lengths. All cables are identical except for length. The HP model number for each cable is as follows:

HP Model No.	Cable Length
10631A	3 feet
10631B	6 feet
10631C	12 feet

2-12   The HP-IB cables use the same piggyback connector on both ends. The connectors may be stacked one on another. As many as 15 instruments (including the controller can be connected in parallel to the same HP-IB, however, the following two restrictions must be observed when piggybacking the HP-IB cables. (1) The total cable length of interconnecting cables for the HP-IB system must be less than or equal to 20 meters (65.6 feet), (2) The total cable length for the system must be less than or equal to 2 meters (6.56 feet) times the total number of devices (e.g., up to 6 meters of cable may be used to connect 3 devices to the HP-IB).

2-13   Multiprogrammer Connector

2-14   All data and control information exchanged between the 59500A and the 6940B passes through MULTI-PROGRAMMER connector (J2) on the rear of the 59500A. Figure 2-2 illustrates the pin configuration of J2 which is a 50 pin microribbon connector. An 18-inch chaining cable (14541A) is supplied with the 59500A to connect the 59500A to the 6940B. A connection is made between pins 18 and 19 of connector J2 through the 59500A unit. This is the system enable (SYE) interlock. Thus, if the cable is removed from J2, all output cards in the system (6940B and any 6941B's) are disabled (refer to Paragraph 3-26 in 6940B manual).

2-15   System Installation

2-16   Procedures for interconnecting a calculator (9830A or 9820A/21A) and a multiprogrammer system (59500A, 6940B, and any 6941B's) to the HP-IB are provided in Chapter IV of the 6940B Multiprogrammer User's Guide. The procedures include connecting the cables, setting addresses, and turning on the equipment in the proper sequence.

2-17 INPUT POWER REQUIREMENTS

2-18   The 59500A may be operated continuously from a nominal 100V, 120V, 220V, or 240V (48-440Hz) power source. A printed circuit board located within the ac power module on the rear panel selects the power source. Voltage choices are available on both sides of the PC board. Before connecting the instrument to the power source, check that the PC board selection matches the nominal line voltage of the source. The operating voltage is shown in the window of the ac power module. If required, select the proper voltage as follows (refer to Figure 2-3):

   a. Remove power cable from instrument.

   b. Move plastic door on power module aside.

   c. Rotate FUSE PULL to the left and remove line fuse F1.

   d. Remove PC board from slot. Select operating voltage by orienting PC board to position the desired voltage on top-left side of PC board. Push board firmly into slot.

   e. Rotate FUSE PULL back into normal position and re-insert fuse F1 in holder using caution to select the correct value for F1 (0.5A slo-blo for 100V or 120V and 0.25A slo-blo for 220V or 240V).

   f. Close plastic door and connect power cable.

2-19   When the instrument leaves the factory, a 0.5A fuse is installed for 120V operation. An envelope containing a 0.25A fuse for 220V/240V operation is attached to the instrument. Make sure that the correct fuse value for F1 is installed if the position of the PC board is changed.

NOTE

The 6940B and 6941B units also have ac power modules on their rear panel. Before connecting these instruments to a power source, ensure that the proper line voltage has been selected and the correct fuse is installed (refer to Section II in the 6940B and 6941B manuals).

2-20   Power Cable

2-21   To protect operating personnel, the National Electrical Manufacturer's Association (NEMA) recommends that the instrument panel and cabinet be grounded. This instrument is equipped with a three conductor power cable. The third conductor is the ground conductor and when the cable is plugged into an appropriate receptacle, the instrument is grounded. The offset pin on the power cable's three prong connector is the ground connection.

Figure 2-1. HP-IB Connector J1
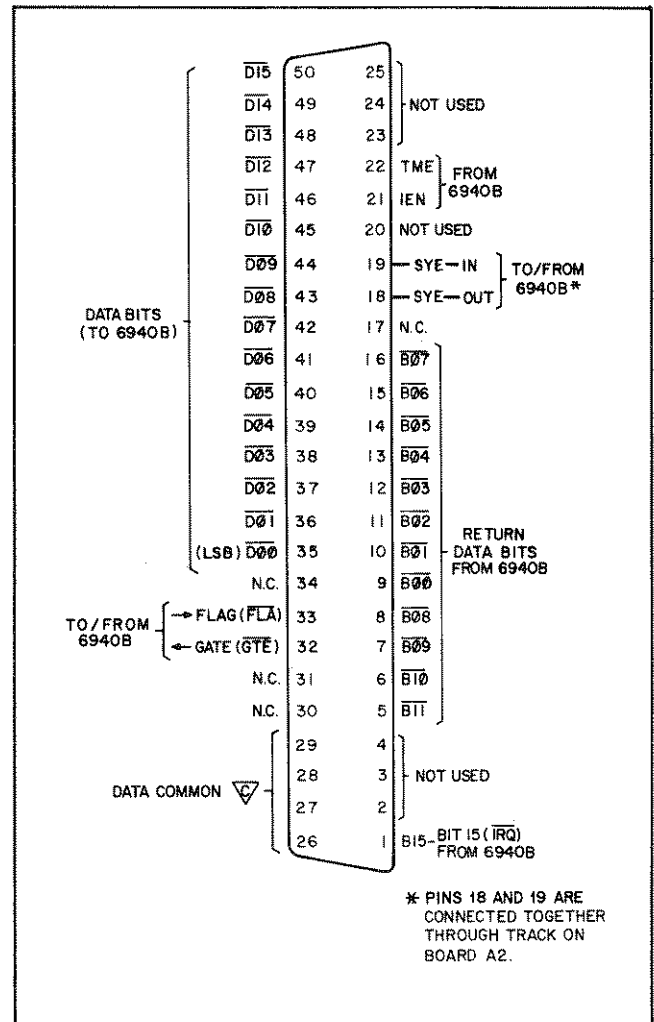
Figure 2-2. Multiprogrammer Connector J2

2-22   To preserve the protection feature when operating the instrument from a two-connect outlet, use a three-prong to two-prong adapter and connect the green lead on the adapter to ground.

POWER MODULE

Operating voltage is shown in module window.

F1

VOLTAGE SELECT
P.C. BOARD
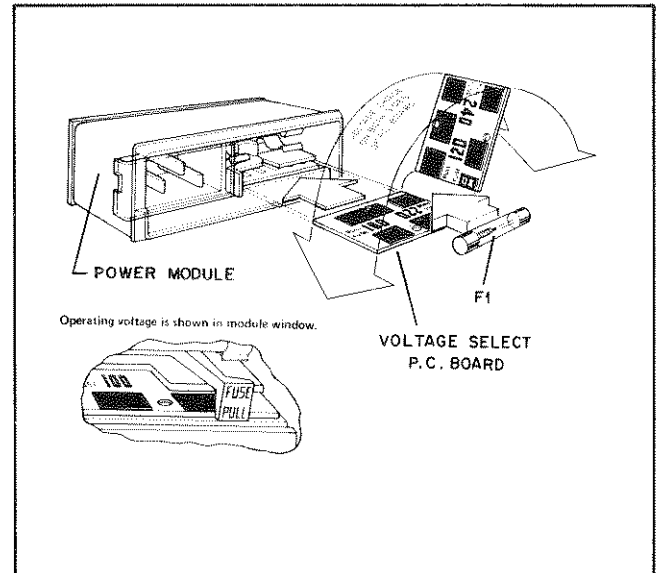
Figure 2-3. Line Voltage Selection

SECTION III
OPERATING INSTRUCTIONS

3-1 PRE-OPERATIONAL CONSIDERATIONS

3-2   Before applying power to the 59500A, ensure that the proper operating voltage (100V, 120V, 220V, or 240V) has been selected and the correct fuse is installed (see Paragraph 2-17). Also, ensure that all HP-IB system connections (between calculator and 59500A, between 59500A and 6940B, and between 6940B and any 6941B's that may be used) have been completed. System cable connections and the power turn-on sequence are described in Chapter IV of the 6940B's User's Guide.

3-3 Controls and Indicators

3-4   **Front Panel.** The 59500A front panel contains an ON-OFF LINE switch (and associated pilot lamp) and six status indicators. The front panel LINE indicator should light and the +5V supply voltage should be present when the LINE switch is turned on. The +5V power supply contains a built-in crowbar to protect the 59500A's circuits (see Figure 7-1, Sheet 1).

3-5   The six status indicators are used in the verification programs and are also useful when troubleshooting the 59500A/6940B multiprogrammer. Four status indicators are associated with the HP-IB-to-59500A interface and two are associated with the 59500A-to-6940B multiprogrammer interface. The function of each indicator is described in Table 3-1.

3-6   **Address Switches.** The talk and listen addresses for the 59500A/6940B are selected by address switches located on the rear of the 59500A Interface Unit. The switches are factory set to correspond with the suggested talk address of "W" and listen address of "7". As shown in Figure 3-1 there are 7 address switches. The last two switches, 6 and 7, have no affect in making the selection and are ignored. The remaining switches, 1 through 5 (corresponding to data lines DIO1 through DIO5) are factory set as follows:

Address Switch	Setting
1	"1"
2	"1"
3	"1"
4	"∅"
5	"1"

3-7   Bits DIO1-DIO5 specify a portion of the address. The complete address is specified by 7 bits (DIO1 through DIO7). The logic states of the two most significant bits DIO7, DIO6) specify a listen or a talk address as follows.

3-8   The listen address "7" is specified by the following logic levels on the HP-IB data lines.

DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1
∅	1	1	∅	1	1	1

LISTEN
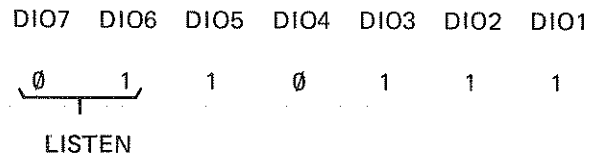
3-9   The talk address "W" is specified by the following logic levels on the HP-IB data lines.

DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1
1	∅	1	∅	1	1	1

TALK
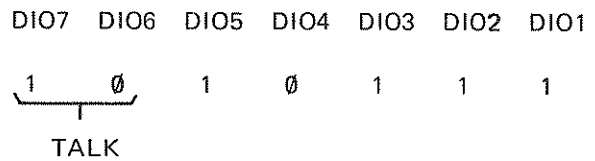
3-10 Pre-Operational Checkout

3-11   The verification programs given in Section V of this manual check that the major functions of the 59500A/6940B multiprogrammer are operational. The verification tests are essentially "GO/NO-GO" checks. If a function is found to be inoperable, troubleshooting procedures are provided to isolate the problem to the 59500A or 6940B. Complete troubleshooting procedures for the 59500A are provided in Section V of this manual while troubleshooting procedures for the 6940B are provided in the 6940B Operating and Service Manual. It is recommended that the verification programs be run when the 59500A/6940B system is first placed in operation.

Figure 3-1. Address Switches on Rear of 59500A

Table 3-1. 59500A Indicators

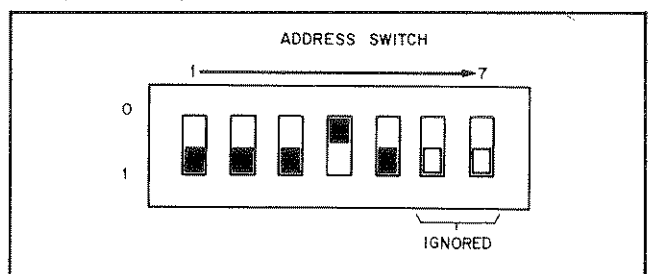| INDICATOR	FUNCTION
LISTEN ADDRESS (HP-IB)	Lights when multiprogrammer is addressed to listen and remains lighted until: 1. Unlisten command is received, or 2. Multiprogrammer talk address is received, or 3. Interface clear signal is received.
TALK ADDRESS (HP-IB)	Lights when multiprogrammer is addressed to talk and remains lighted until: 1. Multiprogrammer listen address is received, or 2. Another bus device is addressed to talk, or 3. Untalk command is received, or 4. Interface clear signal is received.
SERVICE REQUEST (HP-IB)	Lights when: 1. Multiprogrammer completes operation(s) in the timing mode, or 2. Multiprogrammer requests an interruption of the current programming sequence. Remains lighted until the serial poll enable command has been received and the multiprogrammer is addressed to talk. The service request is <u>not</u> reset (SERVICE REQUEST INDICATOR off) in response to the interface clear signal.
SERIAL POLL (HP-IB)	Lights when serial poll enable command (SPE) has been received and multi-programmer is addressed to talk. Remains lighted until: 1. Serial poll disable (SPD) command is received, or 2. Another bus device is addressed to talk, or 3. Untalk command is received, or 4. Interface clear signal is received.
GATE (Multiprogrammer)	Lights when multiprogrammer gate signal is generated and remains lighted until gate signal is terminated. The gate signal can only be generated when a "T" gate code is received. The gate signal is terminated when the leading edge of the multiprogrammer flag is received. Note that the "X" code can be used to terminate the gate signal for certain "hangup" conditions (see Paragraphs 6-37 and 6-57 in 6940B User's Guide).
FLAG (Multiprogrammer)	Lights when multiprogrammer is busy and extinguishes when multiprogrammer is ready to accept new data. During the timing mode there is a wait-for-flag interval that starts (flag busy) when a multiprogrammer input/output card is addressed with a gate ("T") and ends (flag ready) when the card returns the trailing edge of the flag. When the flag goes ready, (in the timing mode), indicating the operation is completed, the SERVICE REQUEST indicator lights.

3-12 OPERATING 59500A/6940B ON THE HP-IB

3-13   The 59500A/6940B is capable of performing the following HP-IB functions: Listener (L4), talker (T6), service request (SR1), acceptor handshake (AH1), and source handshake (SH1). The 59500A/6940B does not have the following HP-IB capabilities: extended listener (LEØ), extended talker (TEØ), controller (CØ), remote-local (RLØ), parallel poll (PPØ), device clear (DCØ), or device trigger (DTØ).

These capabilities (HP-IB compatibility mnemonics L4, T6, LEØ, TEØ, etc.) are defined in IEEE Std. 488-1975 (IEEE Standard Interface for Programmable Instrumentation). The 59500A/6940B HP-IB functions are briefly described in the following paragraphs.

3-14 Listener Function (L4)

3-15   **Conditions for Addressing and Unaddressing.** See LISTEN ADDRESS indicator in Table 3-1.

3-16   Data Input Format. The 59500A converts serial ASCII characters from the HP-IB into the 16-bit format required by the 6940B. Control, data, and address words are received. These formats are described in Paragraphs 5-6 through 5-22 of the 6940B Multiprogrammer User's Guide.

3-17   Talker Function (T6)

3-18   Conditions for Addressing and Unaddressing. See TALK ADDRESS indicator in Table 3-1.

3-19   Data Output Format. The 59500A/6940B sends two types of words to the HP-IB: return data words and status bytes. A return data word contains an input request character, four octal data characters, and carriage return/line feed characters. An 8-bit status byte is sent to the HP-IB in response to a serial poll routine. The formats for return data words and status bytes are descirbed in Paragraph 5-23 through 5-31 of the 6940B Multiprogrammer User's Guide.

3-20   Serial Poll Responses. See SERIAL POLL indicator in Table 3-1.

3-21   Service Request Function (SR1)

3-22   The service request function is used by the 59500A

to notify the controller that the multiprogrammer requires service. The reasons for a multiprogrammer service request are listed in Table 3-1 (SERVICE REQUEST indicator). Refer to Paragraph 3-28 in Chapter III of the 6940B Multiprogrammer User's Guide for a detailed description

3-23   Acceptor Handshake Function (AH1)

3-24   A three-wire handshake cycle occurs with each character transferred from the HP-IB (source) to the 59500A (acceptor). The acceptor handshake cycle is described in detail in Paragraph 4-3 of this manual.

3-25   Source Handshake Function (SH1)

3-26   A three-wire handshake cycle occurs with each character transferred from the 59500A (source) to the HP-IB (acceptor). The source handshake cycle is described in detail in Paragraph 4-13 of this manual.

3-27   PROGRAMMING

3-28   Complete programming instructions are provided in Chapters V and VI of the 6940B User's Guide. Chapter V contains programming fundamentals and Chapter VI contains sample programs for each type of plug-in card that can be used in the multiprogrammer mainframe.

SECTION IV
PRINCIPLES OF OPERATION

4-1 INTRODUCTION

4-2 This section describes the 59500A's 3-wire hand-shake timing circuits that control the transfer of each character between the HP-IB and the 59500A. Descriptions and timing diagrams are provided for the acceptor hand-shake circuits (HP-IB-to-59500A transfers) and for the source handshake circuits (59500A-to-HP-IB transfers). The descriptions and diagrams support the troubleshooting procedures provided in Section V. The remaining circuits (decoders, latches, etc.) within the 59500A are described in sufficient detail in Chapter III of the 6940B Multipro-grammer User's Guide to support the troubleshooting procedures given in this manual.

4-3 ACCEPTOR HANDSHAKE

4-4 The acceptor handshake circuits consist of the 3-wire handshake logic, clock generator and the acceptor handshake logic (see Figure 7-1, Sheet 2). When the HP-IB is in the command mode ($\overline{\text{ATN}}$ true) or when the 59500A is in the listen mode (addressed to listen and $\overline{\text{ATN}}$ goes false), the 3-wire handshake logic is enabled through NOR gate Z53. As each character is transferred to the 59500A (acceptor) from the controller (source), a 3-wire handshake cycle occurs. Unrecognized characters will be ignored (not decoded) but the handshake cycle will occur anyway. The timing sequence for the handshake cycle depends upon a number of conditions which are described in the following paragraphs. Timing diagrams are included with each description. Note that the encircled numbers on the timing diagrams designate test points which coincide with the test points shown on the schematic and component location diagrams provided in Section VII.

4-5 All Characters Except "T", "X", And "Z"

4-6 Figure 4-1 illustrates the timing sequence when any character except a "T", "X", or "Z" gate code is received by the 59500A.

T_0: Initially, the $\overline{\text{NRFD}}$ signal (J1-7) is HI (false-ready for data) and the $\overline{\text{NDAC}}$ signal (J1-8) is LO (true-data not accepted). Also $\overline{\text{DAV}}$ (J1-6) is HI (false-data not valid) at this time.

T_1: The source (assume controller) puts a character on the HP-IB and indicates that the character is valid by setting $\overline{\text{DAV}}$ LO (true).

T_2: After a delay of approximately $0.3\mu\text{sec}$, the CLKL (Z62-13) and $\overline{\text{CLKL}}$ (Z62-4) signals are generated.

a. If the HP-IB is in the command mode ($\overline{\text{ATN}}$ LO), the CLKL signal gates a recognized command character which sets or resets the applicable latch (listen, talk or serial poll).

b. If the 59500A has been previously commanded to listen and $\overline{\text{ATN}}$ goes HI (false), the CLKI signal (Z54-11) is generated and gates a recognized number into the output data shift register (Z18-Z20) or a recognized letter (other than "T", "X", "Z") into the address register (Z17).

T_3: After approximately $0.5\mu\text{sec}$, the trailing edge of $\overline{\text{CLKL}}$ signal (Z62-4) sets NDACL flip-flop (Z49). With Z49 set, the $\overline{\text{Q}}$ output (Z49-8) goes LO causing $\overline{\text{NRFD}}$ (J1-7) to go LO (not ready for data) and $\overline{\text{NDAC}}$ (J1-8) to go HI (data accepted).

T_4: The controller, sensing $\overline{\text{NDAC}}$ HI, sets $\overline{\text{DAV}}$ HI (data not valid). With $\overline{\text{DAV}}$ HI, DACL flip-flop Z49 is cleared causing $\overline{\text{NDAC}}$ (J1-8) to go LO (data not accepted). Also with DACL F/F cleared (Z49-8 HI), input pin 1 to NAND gate Z63 is HI. Input pins Z63-2 and 13 are also HI in this case (any character except "T", "X", or "Z") causing $\overline{\text{NRFD}}$ to go HI (ready for data). At this point, the handshake cycle is completed allowing the controller to initiate another transfer.

4-7 "T", "X", Or "Z" Characters

4-8 Figure 4-2 illustrates the timing sequence when an "X" or "Z" gate code, or a "T" gate code (with TME off) is received. The timing sequence is the same as described in Paragraph 4-6 except that at T_4, the $\overline{\text{NRFD}}$ signal is held LO (not ready for data) preventing the controller from inputting another character for approximately $30\mu\text{sec}$. The delay allows the 6940B sufficient time to store and process the data that preceded the gate code character. The $30\mu\text{sec}$ delay is provided by gate code detector Z64 which holds Z63-2 LO for approximately $30\mu\text{sec}$. After $30\mu\text{sec}$, (see T_5, Figure 4-2), $\overline{\text{NRFD}}$ goes HI (ready for data).

4-9 As shown in Figure 4-2, the "T" code generates the multiprogrammer gate which strobes bits $\overline{\text{D00}}$ through $\overline{\text{D15}}$ into the 6940B and also results in an automatic flag (J2-33) from the 6940B when the timing mode is off (TME at J2-22 is LO). The trailing edge of the flag generates a $2\mu\text{sec}$ positive pulse (Z62-5) which stores return data bits ($\overline{\text{B11}}$-$\overline{\text{B00}}$) in the input latch (Z14-Z16). The trailing edge of the flag also generates a $2\mu\text{sec}$ negative pulse (Z62-12)

which is used to set $\overline{SRQ}$ (J1-10) LO (true) when the 6940B is in the timing mode (see Paragraph 4-11).

4-10 "T" Character With TME On

4-11 When a "T" is received and the 6940B is operating in the timing mode (TME at J2-22 is HI), the timing sequence is the same as shown in Figure 4-2 except that the $\overline{NRDF}$ signal can be held LO (not ready for data) for more than 30μsec. In the timing mode, Z63-13 is held LO by the flag signal. If the 6940B does not complete operations within 30μsec, the flag signal will override the gate code delay (see Figure 4-2, T_5). In many cases the flag will be held LO for a number of seconds until the 6940B completes operations. When operations are completed, the trailing edge of the flag will cause $\overline{NRFD}$ to go HI (ready for data). With TME on, the trailing edge of flag also sets the service request ($\overline{SRQ}$) LO indicating that operations are completed.

4-12 Note that the 6940B flag signal will not affect the $\overline{NRFD}$ handshake signal when the 6940B is in the interrupt mode ($\overline{IEN}$ and TME both on). For this condition, the inputs at pins 12 and 13 of NAND gate Z56 are both HI. Consequently, the output (pin 6) of NAND gate Z63 is HI overriding the flag input at pin 3 of Z63. Thus, when multiprogrammer input card(s) time out (interrupt), the resulting flag(s) will not affect the $\overline{NRFD}$ line, however, the trailing edge of the flag from the first interrupting card sets the $\overline{SRQ}$ line true (LO).
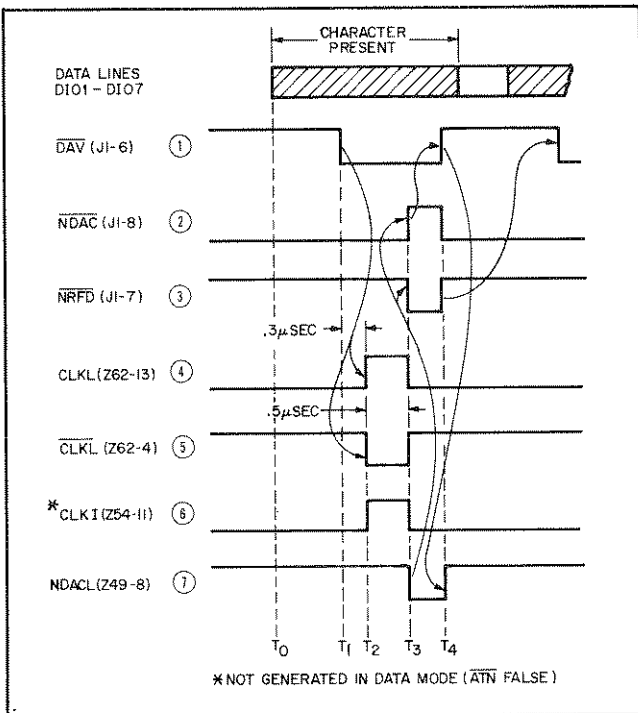

Figure 4-1. Acceptor Handshake Signals (All Characters Except "T", "X", and "Z") Timing Diagram

4-13 SOURCE HANDSHAKE

4-14 A 3-wire handshake cycle occurs with each character transferred from the 59500A (source) to the controller (acceptor). The source handshake logic implements the handshake cycle and also advances the encoder sequencer as each character is transferred (see Figure 7-1, Sheet 2).

4-15 When the 59500A talk address is received and $\overline{ATN}$ goes false (HI), the encoder will translate bit $\overline{MB15}$ into one octal digit and bits $\overline{MB11}$-$\overline{MB00}$ into four octal digits. The octal digits (characters) are transmitted from the encoder onto the HP-IB starting with the octal digit representing $\overline{MB15}$, followed by four octal digits representing $\overline{MB11}$-$\overline{MB09}$, $\overline{MB08}$-$\overline{MB06}$, $\overline{MB05}$-$\overline{MB03}$, and $\overline{MB02}$-$\overline{MB00}$, respectively. Carriage return (CR) and line feed (LF) characters are added after the last octal digit ($\overline{MB02}$-$\overline{MB00}$) as an "end of record" indication to the controller.

4-16 The first character (representing $\overline{MB15}$) is enabled and transferred onto the bus as soon as the 59500A's talk address is received and $\overline{ATN}$ goes false. The remaining characters are enabled and transferred with each subsequent
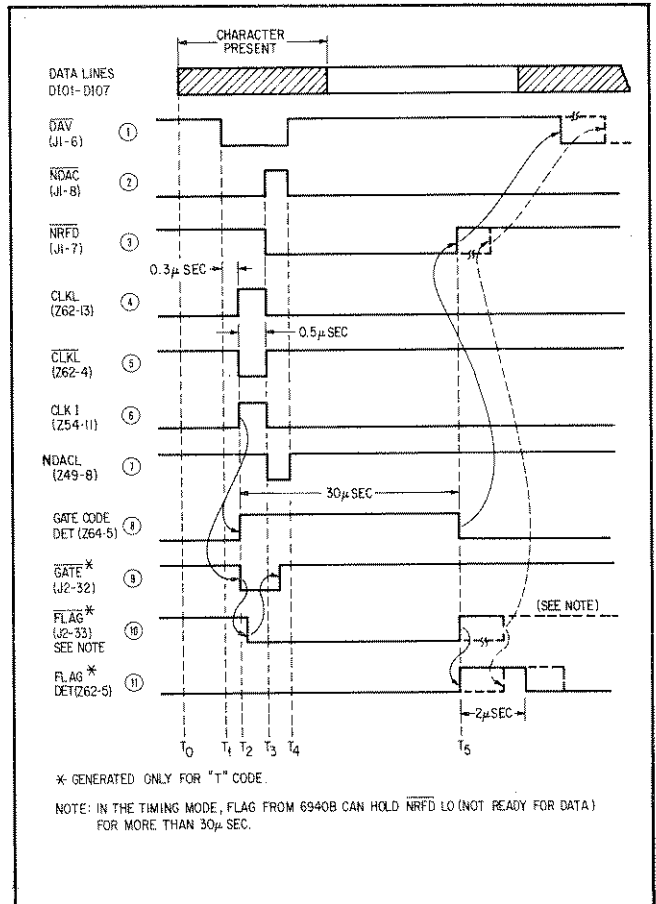

Figure 4-2. Acceptor Handshake Signals ("T", "X", or "Z" Characters) Timing Diagram

handshake cycle. Since the controller (in this case calculator) ends the input cycle after the CR/LF characters are received, the transfer is terminated and the encoder sequencer is cleared after the seven characters have been transferred. Note that if the cycle is not terminated, these seven characters plus nine "7's" would be transferred. Thus, if the bus handshake is continued, the 59500A will repeatedly send a string of 16 characters.

4-17   The timing sequence that occurs with each character transferred is shown in Figure 4-3.

T_0: Initially, the 59500A is addressed to talk, $\overline{ATN}$ is false (HI), and the listener (controller in this case) is ready for data: $\overline{NRFD}$ goes HI and $\overline{NDAC}$ is LO.

T_1: After a delay of approximately 4μsec, Z57-5 goes HI causing a negative pulse (approx. 2μsec wide) to be generated at Z64-4. See source handshake circuits on Sheet 2 of Figure 7-1.

T_2: The trailing edge of the 2μsec negative pulse from Z64-4 causes Z57-9 (DAVT) to go HI and Z57-8 ($\overline{DAVT}$) to go LO. With DAVT HI, $\overline{DAV}$ goes LO indicating that the character is valid.

T_3: With $\overline{DAV}$ LO, the controller (acceptor) sets NDAC HI (data accepted) and $\overline{NRFD}$ LO (not ready for data). With $\overline{NDAC}$ HI, Z57-5 goes LO, Z57-9 goes LO, and Z57-8 goes HI. With Z57-9 LO, $\overline{DAV}$ goes HI indicating the character is not valid. The LO to HI transition at Z57-8 advances the encoder sequencer enabling the next character to be transferred (see Paragraph 4-18).

T_4, T_5: The listener sets $\overline{NDAC}$ LO and NRFD HI and the cycle is repeated (see T_1).

4-18   The encoder sequencer consists of the following: 4-bit up counter (Z47), 4-to-10 line decoder (Z48), and inverters (Z41, Z45, and Z54). These circuits provide the enable signals that transfer the seven characters in the proper order. The up counter (Z47) is cleared when the 59500A is not enabled to talk or when $\overline{ATN}$ is true. For this condition, EN1 is HI, enabling encoder bit $\overline{MB15}$. When the 59500A is addressed to talk and $\overline{ATN}$ goes false, the first character (representing bit MB15) is transferred. Each character is then transferred in succession under con-

trol of the handshake cycle. As each character is accepted, the up-counter is advanced by one and the 4-to-10 line decoder (Z48) produces the next enable signal (EN2, EN3, EN4, etc.). The combination of enable signals and encoder gates and inverters produces the proper ASCII code on data lines DIO1-DIO7 for each character transferred.

4-19   Note that when the serial poll enable latch (Z40) is set, the 59500A is addressed to talk, and $\overline{ATN}$ goes false, a low level pulse ($\overline{LD}$) is generated and loads a count of 4 into the 4-bit up-counter (Z47). For this condition, enable service byte (ENSB) is HI since both EN5 and serial poll active state (SPAS) are both high. The ENSB signal is NANDed (Z39) with the service request active state (RQSA) signal, encoded as bit DIO7, and transferred along with DIO1-DIO6 as the status byte.
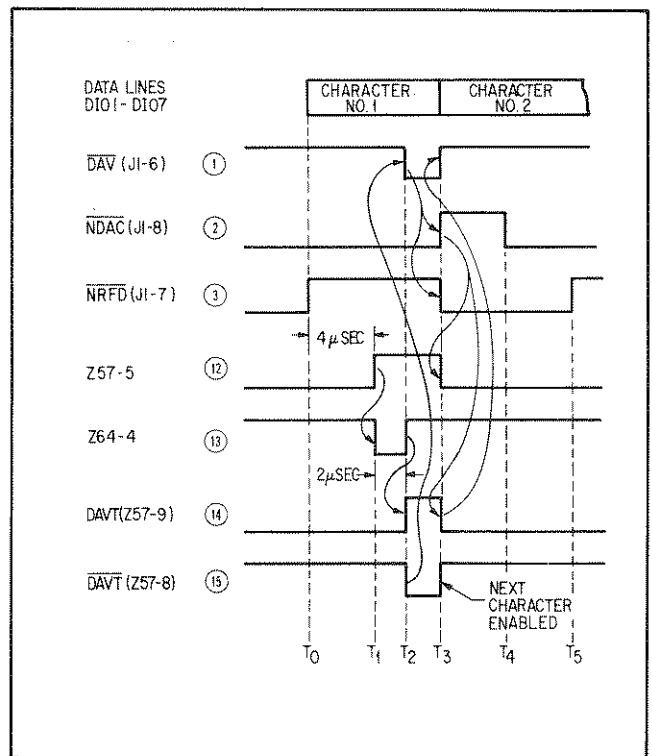

Figure 4-3. Source Handshake Signals, Timing Diagram